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A systematic investigation of the degradation mechanisms in SOI n-channel LD-MOSFETs

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Abstract

The operation and degradation mechanisms in silicon on insulator LD-MOSFETs are governed by the series resistance which is back-gate bias dependent. The influence of the back-gate bias during degradation and subsequent testing is investigated and modeled. The damage formation and overall loss in LD-MOSFETs performance induced by irradiation, hot-carrier injection, or low temperature are complex and remarkably different from the more usual case of low-voltage CMOS transistors. The series resistance can change by a factor of 4 according to the back-gate bias and radiation dose. The degradation processes are clearly identified and the main parameters (oxide charges, traps at the front and back interfaces, series resistances) are extracted using a simple model of the LD-MOSFET, which accounts for the modification of the drift region resistance.

Keywords: LD-MOSFET; SOI; Irradiation; Hot-carrier degradation; Low temperature; Breakdown voltage; Series resistance

1. Introduction

Silicon on insulator (SOI) technology is successfully entering the competitive market of low-voltage, high-performance integrated circuits. But there is also great interest in utilizing SOI lateral double-diffused MOSFETs (LD-MOSFETs) (Fig. 1) for mid-voltage, high-voltage and RF integrated circuits as well as for voltage conversion and space applications [1–4]. SOI offers several distinct advantages: (i) lateral inter-device isolation and vertical isolation of the high-doped, thin silicon film from the low-doped substrate, (ii) immunity to transient radiation effects, (iii) wide range of operating temperature, (iv) possibility to adjust the thickness of the Si film and buried oxide (BOX), (v) high breakdown voltage by controlling the parasitic bipolar transistor, etc. [5].

The wafer substrate can be biased to create an accumulation, depletion, or inversion layer at the back interface of the film (between the thin silicon layer and BOX). This 'back-gate bias' modulates the series resistance of the drift region and, simultaneously, can activate the back-channel conduction, hence modifying the overall device performance (current drive, on-resistance, transconductance, leakage current, breakdown voltage) [6–8]. During device degradation, by irradiation or hot-carrier injection, defects are created in different locations and alter the flat-band voltage and threshold voltage at the front/back interfaces, the carrier mobility, and the series resistance. These parameters are also modified in

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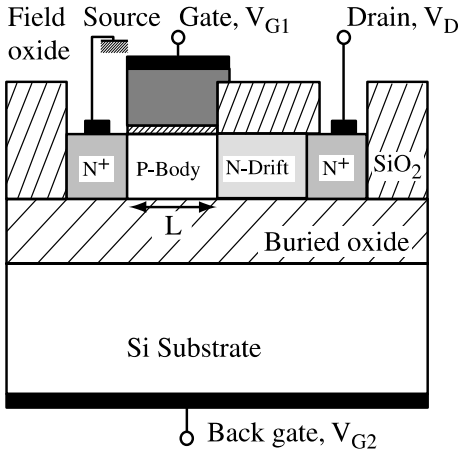

Fig. 1. Cross-section of an n-channel LD-MOSFET fabricated on SOI.

low-temperature operation, such as in space applications.

The purpose of this work is to examine, for the first time, the signature of the degradation mechanisms, which is the base for further optimization of SOI LD-MOSFETs intended for operation in harsh conditions. In Section 2, we discuss the experimental characteristics for the front and back channels of the LD-MOSFET and explain the influence of the back-gate bias. In Section 3, a comprehensive model [8], which is necessary for understanding the device degradation and for extracting the relevant parameters, is briefly reviewed. Finally, irradiation, hot-carrier injection, and low-temperature degradation results are examined in Section 4.

2. Device characteristics

2.1. Device description

The typical structure of an n-channel LD-MOSFET is schematically illustrated in Fig. 1. The devices were fabricated with standard partially depleted 0.35 μm CMOS/SOI technology, by varying the parameters of the SOI wafers. In particular, the thickness ranges for the gate oxide, silicon film, and BOX were respectively $t_{ox1} \approx 7$–10 nm, $t_{Si} \approx 100$–300 nm, and $t_{ox2} \approx 200$–500 nm. The p-type channel and n-type drift regions were both 4 μm long. The source was tied to the body to avoid transient and floating body effects. The doping profile was tailored for achieving a breakdown voltage roughly ranging from 18 to 20 V.

2.2. Front-channel characteristics

In linear operation ($V_D = 100$ mV), the drain current I_D and transconductance g_{m1} curves (Fig. 2a and b) versus front-gate voltage (V_{G1}), exhibit a remarkable dependence with back-gate bias, V_{G2}. Three different regions of operation can be distinguished in Fig. 2 and were explained earlier [8]:

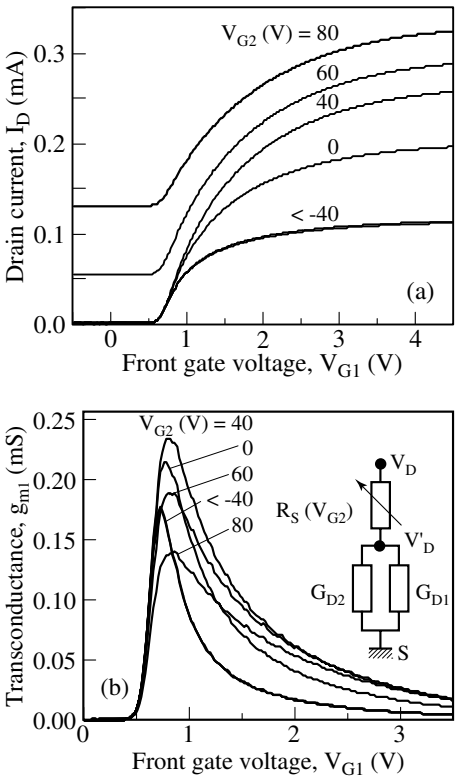

Fig. 2. (a) Drain current and (b) transconductance versus front-gate voltage with back-gate voltage as a parameter (n-channel LD-MOSFET, $V_D = 100$ mV). The inset shows the equivalent circuit of the LD-MOSFET.

- *Region 1* ($V_{G2} < -40$ V): The back interface in the transistor body is accumulated and the bottom of the drift region is inverted. There is no back-channel conduction and the depletion width in the drift region is maximum. The series resistance, determined by the undepleted part of the drift region, is constant and maximum. The $I_D(V_{G1})$ and $g_m(V_{G1})$ characteristics do not change with V_{G2}.
- *Region 2* ($-40 < V_{G2} < +50$ V): The back channel is still off, whereas the depletion depth in the drift region shrinks with increasing V_{G2}. The front-channel current in strong inversion and the transconductance peak both increase with increasing V_{G2} simply because the drift region becomes less and less resistive.
- *Region 3* ($V_{G2} > +50$ V): When the back-gate voltage exceeds the back-channel threshold voltage V_{T2}, the film–BOX interface in the body becomes strongly inverted. The back-channel current is added to the

front-channel current. The contribution ΔI_D of the back channel is constant only when the front channel is off (for $V_{G1} < 0.5$ V) and gradually decreases as the front-channel inversion becomes stronger. This effect can be understood with the help of the equivalent circuit (inset in Fig. 2b), by noticing that an increasing front-channel current augments the voltage drop on the series resistance which, in turn, reduces the effective drain voltage (V'_D): the extra current ΔI_D supplied by the back channel therefore decreases. Similarly, the effective bias V'_D is also reduced as V_{G2} increases beyond 50 V; this is why the front-channel transconductance peak is degraded with V_{G2} (Fig. 2b) in spite of the fact that the film–BOX interface is strongly accumulated in the drift region and the series resistance is lower.

2.3. Back-channel characteristics

The back-channel curves $I_D(V_{G2})$ and $g_{m2}(V_{G2})$ are measured by reversing the roles of the front and back gates. There is no modulation of the series resistance by the front-gate bias because the field oxide, which covers the drift region, is too thick. For a strongly inverted front channel (for example, pre-rad curves at $V_{G1} =$ 1.5–2 V in Fig. 6b), it is observed that the drain current increases with V_{G2} *even when the back channel is off*. This intriguing behavior is due to the reduction in series resistance $R_s(V_{G2})$ which now increases V'_D bias. This effect is reflected by an unusual shoulder in transconductance (for $V_{G2} < +45$ V in Fig. 3): the back-gate transconductance g_{m2} is non-zero when the back channel is blocked because it accounts for the variation of the front-channel current with V_{G2}. On the other hand, the back-channel transconductance peak starts to dramatically degrade as soon as the front channel is activated and lowers V'_D bias.

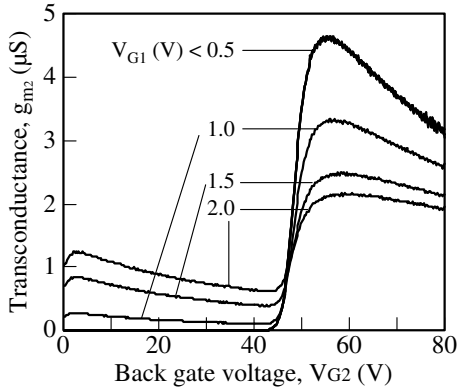

Fig. 3. Back-gate transconductance versus back-gate voltage with front-gate voltage as a parameter (n-channel LD-MOSFET, $V_D = 100$ mV).

3. Model

3.1. Conductance and transconductance

An LD-MOSFET can be represented by the simple equivalent circuit shown in Fig. 2b [8,9]. $R_s(V_{G2})$ is the resistance of the drift region, and $G_{D1,2}$ are the *pure* conductances (i.e., free of any series resistance effects) of the independent front (subscript 1) and back (subscript 2) channels given by

$$G_{D1,2} = \frac{\mu^0_{1,2} C_{ox1,2} W/L}{1 + \theta^0_{1,2}(V_{G1,2} - V_{T1,2})}(V_{G1,2} - V_{T1,2}) \quad (1)$$

where μ^0 is the electron mobility, C_{ox} is the oxide capacitance, W is the channel width, and L is the channel length. The mobility attenuation coefficient θ^0 depends on the thickness of the corresponding oxide, not on R_s. The total drain current is given, for double channel conduction, by

$$I_D = \frac{G_{D1} + G_{D2}}{1 + (G_{D1} + G_{D2})R_s} V_D \quad (2)$$

Device degradation results in a modification of the threshold voltages $V_{T1,2}$, carrier mobilities, and series resistance. However, neither the back-channel conductance G_{D2} nor the series resistance depend on V_{G1} because (i) the transistor is partially depleted and (ii) the field oxide above the drift region is very thick. Hence, the front-gate transconductance is easily derived:

$$g_{m1} = \frac{\partial G_{D1}/\partial V_{G1}}{[1 + (G_{D1} + G_{D2})R_s]^2} V_D \quad (3)$$

3.2. Parameter extraction

The experimental results described in Section 2 can all be explained by injecting appropriate parameters in the equivalent circuit. It is worth keeping in mind that the intrinsic drain voltage V'_D depends on front- and/or back-gate bias in two distinct ways: (i) modulation of the series resistance $R_s(V_{G2})$ and (ii) change in voltage drop on R_s when a second channel is activated at the front or back interface.

The parameters of the model (i.e. carrier mobility, threshold voltage, R_s) are extracted, as in low-voltage SOI MOSFETs, by applying the method based on the $I_D/\sqrt{g_m}$ ratio [5,10] to the front channel operated alone (Fig. 4a). When the variation of $R_s(V_{G2})$ is weak, the same procedure can be repeated for the back channel.

In the case of *double channel* conduction, the method should be revised due to the back-channel current and variable series resistance $R_s(V_{G2})$. In a first step, combining Eqs. (1)–(3) yields [8]

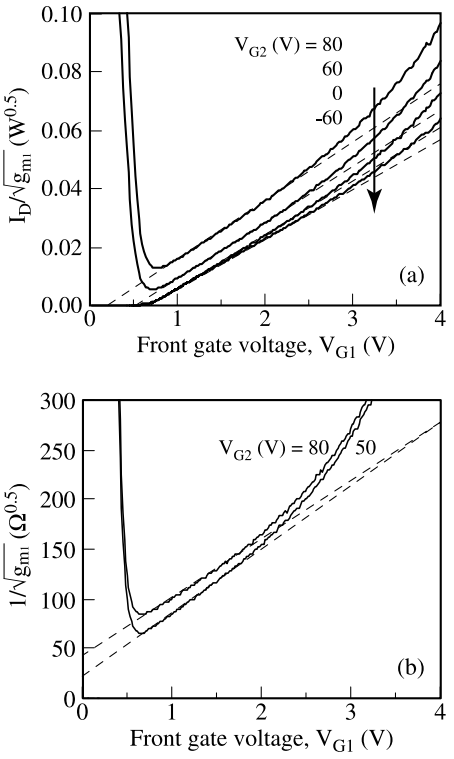

Fig. 4. Experimental variation of (a) $I_D/(g_m)^{0.5}$ and (b) $1/(g_m)^{0.5}$ versus front-gate voltage with back-gate voltage as a parameter. The dotted lines indicate the best linear fits (LD-MOSFET).

$$\frac{I_D}{\sqrt{g_{m1}}} = \frac{V_D}{A}(G_{D1} + G_{D2})[1 + \theta_1^0(V_{G1} - V_{T1})] \quad (4)$$

where $A = \sqrt{\mu_1 C_{ox1} V_D W/L}$. The coefficient θ_1^0 can be neglected

$$\frac{I_D}{\sqrt{g_{m1}}} \cong A(V_{G1} - V_{T1}) + \frac{V_D}{A} G_{D2} \quad (5)$$

which means that the second term in Eq. (5) is rather insensitive to V_{G1}.

In Fig. 4a, the slope A of the extrapolated straight line, $I_D/\sqrt{g_{m1}}$ vs. V_{G1}, is governed by the front-channel mobility. The intercept with the horizontal axis depends on G_{D2} (function of V_{G2} and R_s) and does not provide the threshold voltage. The curves of Fig. 4a are parallel and their slopes are rather independent on R_s.

In a second step, we rewrite Eq. (3) as

$$\frac{1}{\sqrt{g_{m1}}} = \frac{1}{A}[1 + \theta_1^0(V_{G1} - V_{T1})][1 + R_s(G_{D1} + G_{D2})] \quad (6)$$

and replace G_{D1}

$$\frac{1}{\sqrt{g_{m1}}} = \frac{A}{V_D} R_s(V_{G1} - V_{T1}) + \frac{1}{A}[1 + \theta_1^0(V_{G1} - V_{T1})][1 + R_s G_{D2}] \quad (7)$$

Neglecting again θ_1^0 yields a straight line, $1/\sqrt{g_{m1}}$ vs. V_{G1}, with a slope proportional to R_s (Fig. 4b) [8]. In summary, the revised method for double-channel conduction consists in determining first μ_1 from the slope of Eq. (5) and then R_s from the slope of Eq. (7).

By contrast with the single-channel method (where $G_{D2} = 0$ for depletion or accumulation at the back interface), in double-channel conduction regime the threshold voltage V_{T1} cannot be extracted from the horizontal intercept of $I_D/\sqrt{g_{m1}}$ line. The activation of the back channel also disqualifies other methods, such as the linear extrapolation of $I_D(V_{G1})$ curves or the constant-current definition of V_{T1}. Instead, the peak of d^2I_D/dV_{G1}^2 does not shift with back-gate bias, and can be used to define the threshold voltage: $V_{G1} = V_{T1}$ at the inflection point in $g_{m1}(V_{G1})$ curve [5,11]. Another indirect approach is to extract V_{T1} from low-voltage MOSFETs (where $R_s \approx 0$), located in the same chip. More details about the model and extraction techniques were given elsewhere [8].

Applying the above methods, we obtain for the front-channel LD MOSFET: threshold voltage $V_{T1} = 0.64$ V, electron mobility $\mu_1 = 450$ cm^2/V s, and subthreshold swing $S_1 = 86$ mV/dec. These values are very close to those extracted in a low-voltage MOSFET. At the back channel, the subthreshold swing ($S_2 = 1.7$ V/dec) and threshold voltage ($V_{T2} = 49$ V) are much higher and the mobility ($\mu_2 = 370$ cm^2/V s) slightly lower. The series resistance, viewed from the front channel, decreases by a factor of 3 from inversion (region 1) to accumulation (region 3) at the back interface of the drift zone (Fig. 7). For flat-band condition ($V_{G2} \approx +20$ V), we obtain $R_s \approx 280\ \Omega$.

4. Degradation mechanisms

4.1. Irradiation

The devices were irradiated with γ-rays up to 1 Mrad (^{60}Co source, rate 2.5–6 rad/s) while keeping $V_S = V_D = 0$ V, $V_{G1} = 4$ V and $V_{G2} = 60$ V. Positive voltage on the front and back gates represents a worst-case bias condition. The positive charge generated in the oxide stands as the major radiation-induced defect. These positive charges are pushed towards the film–oxide interfaces, where their effect on the channel conduction is obviously maximized.

The degradation of the thin, high-quality front-gate oxide was marginal. The subthreshold slope only slightly increased with dose, from 86 to 100 mV/dec which cor-

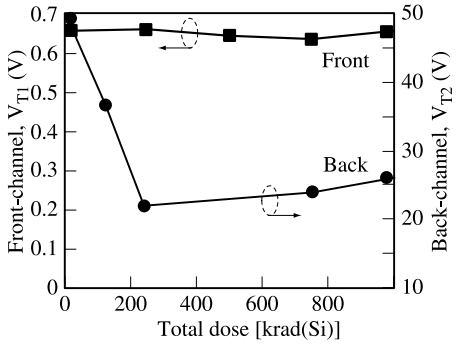

Fig. 5. Back- and front-channel threshold voltage variation with total dose in a LD-MOSFET.

responds to the formation of 2×10^{11} cm^{-2} eV^{-1} interface traps. The threshold voltage (determined in regions 1 and 2 where $G_{D2} = 0$) did not change significantly. The real radiation effect was the trapping of a large amount of positive charge (2×10^{12} cm^{-2}) in the BOX. This caused a strong decrease in series resistance and a negative 30–40 V shift in back-channel threshold voltage (Fig. 5). For a dose in excess of 250 krad, V_{T2} tends to slightly increase (turn-over) reflecting a relative saturation of the trapped charge as well as the generation of back-interface traps.

After irradiation, the modulation of the front-interface characteristics $I_D(V_{G1})$ with V_{G2} in region 2 is still visible in Fig. 6a but substantially reduced; the curves are closer to each other due to a narrower range of R_s (Fig. 7). Our extraction methods confirm that the series resistance, measured at negative V_{G2}, exhibits a sharp decrease with total dose: for $V_{G2} = -40$ V, R_s drops by a factor of 3 after 1 Mrad exposure (Fig. 7). In other words, a moderately high, negative V_{G2} is no longer sufficient to deplete the drift region, which remains accumulated due to the large amount of positive charge in the BOX. Fig. 7 shows that after 250 krad exposure, the series resistance becomes rather independent of back-gate bias and prevents the LD-MOSFET from operating in regions 1 and 2. Note that the positive charge trapped in the field oxide, above the drift region, also contributes to the reduction of R_s.

The variation of the front-channel transconductance peak with total dose and V_{G2} as a parameter is illustrated in Fig. 8. These curves seem to look inconsistent because opposite trends are observed, according to the back-gate bias used in the measurement. For $-60 \leqslant V_{G2} \leqslant +20$ V, the transconductance peak surprisingly *increases* (by up to 25% for $V_{G2} = -40$ V) with total dose and saturates above 500 krad. This measurement is neither wrong, nor should it be naively attributed to an improvement of mobility with dose. The increase in g_m peak is simply related to the gradual reduction of the series resistance

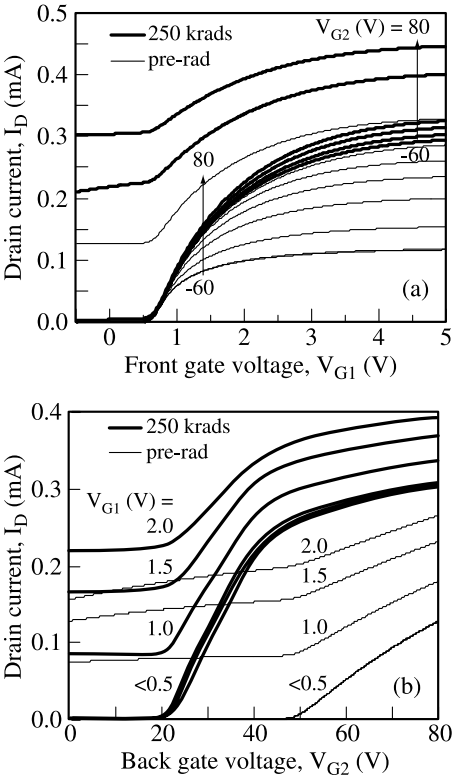

Fig. 6. Drain current versus (a) front-gate voltage and (b) back-gate voltage before and after irradiation. The bias applied to the opposite gate is a parameter (n-channel LD-MOSFET, V_D = 100 mV).

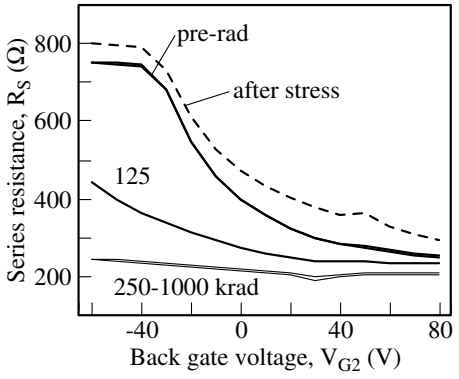

Fig. 7. Series resistance evolution with back-gate bias after various total doses of radiation and after back-channel stress at $V_{G2} = 80$ V (dotted curve).

during the buildup of positive charges in the buried oxide.

An opposite variation is measured for $V_{G2} \geqslant 40$ V: the transconductance decreases with dose and saturates

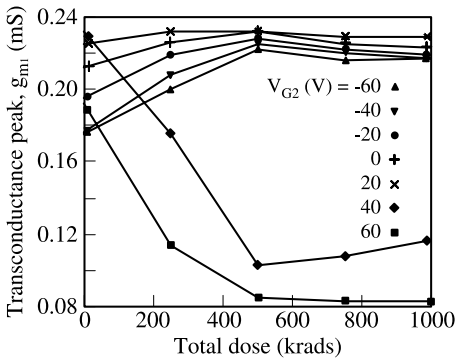

Fig. 8. Front-channel transconductance peak versus total radiation dose in an n-channel LD-MOSFET. The tests were conducted with various back-gate bias and $V_D = 100$ mV.

above 500 krads. Again, the transconductance drop does not reflect the real mobility degradation which is actually limited to less than 10% even after 1 Mrad. Due to the onset of the back-channel conduction, the effective drain voltage, V'_D, decreases, according to $V'_D = V_D - R_s(I_{D1} + I_{D2})$. As dose increases, V_{T2} decreases (Fig. 6), raising the back-channel current and also the voltage drop across the series resistance. V'_D and the transconductance are therefore reduced and tend to saturate above 500 krad when V_{T2} saturates too. We conclude that in LD-MOSFETs the modulation of V'_D, R_s and back-channel current govern the transconductance behavior during irradiation and can offset the effect of a mobility degradation at the front channel.

The back-channel characteristics $I_D(V_{G2})$ with V_{G1} as a parameter are plotted in Fig. 6b. The curves are shifted to the left as a consequence of the large reduction in back-channel threshold voltage due to positive charge trapping in the BOX. Note that the back-channel mobility and subthreshold swing are also significantly degraded after exposure to a high dose of radiation. However, the transconductance is improved after radiation (at 250 krad, Fig. 6b) due to the lowering of the series resistance which prevails over the degradation in mobility.

The overall radiation effect in LD-MOSFETs under normal front-gate operation is an increase in drain current with dose, induced in particular by the change in V_{T2} and, for low (negative) back-gate bias, by the decrease in series resistance.

4.2. Hot-carrier injection into the BOX

The devices were stressed by keeping the *back channel* in strong inversion ($V_{G2} = 80$ V, i.e., accumulated drift region) and grounding the front gate. The stress was performed with $V_D = 15$ V for 2000 s. The degradation is dominated by electron injection from the back channel into the BOX where they get trapped. This mechanism moderately alters, by less than 10%, the current and the transconductance of the back channel. Since the threshold voltage V_{T2} is not shifted, the change in transconductance is presumably due to the increase in series resistance. The subthreshold slope S_2 is not degraded which indicates only a minor generation of fast traps at film–BOX interface.

The front-channel curves were clearly modified (Fig. 9a) although none of the front-interface parameters was actually degraded (V_{T1}, μ_1, S_1). The decrease in drain current is accentuated when the back channel is activated ($V_{G2} \geqslant 50$ V) and more so in strong inversion (10–15% for $V_{G1} = 4$ V) than below threshold ($V_{G1} \leqslant 0.5$ V). This behavior is typical for an *increase* in series resistance and a decrease in back-channel transconductance. Such a situation is therefore perfectly opposite to the case of irradiation. The extracted series resistance exhibits an approximately constant increase for the entire range of back-gate bias (dotted line in Fig. 7). This is why the degradation effect appears more clearly in post-stress tests performed in regions 2 and 3, where the

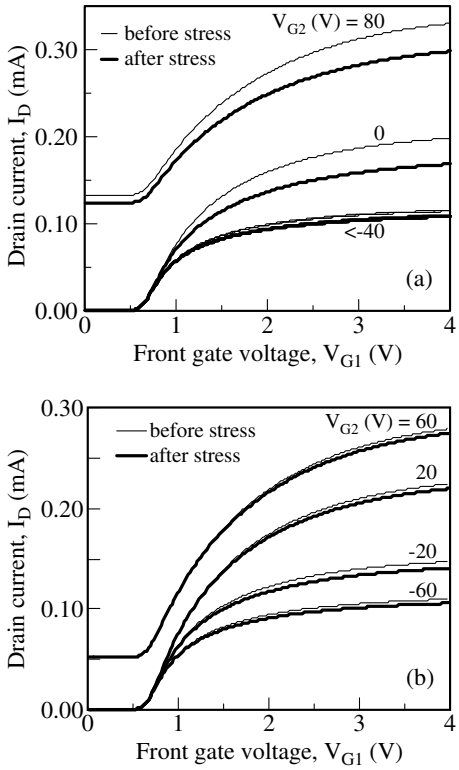

Fig. 9. Modification of the drain current versus front-gate voltage after (a) back channel stress ($V_{G1} = 0$ V, $V_{G2} = +80$ V, and $V_D = 15$ V) and (b) front-channel stress ($V_{G1} = 3$ V, $V_{G2} = 0$ V, and $V_D = 19$ V). The back-gate voltage was a further parameter during post-stress tests (LD-MOSFET, $V_D = 100$ mV).

initial value of the series resistance is lower and the ratio $\Delta R_s/R_s$ is higher.

The modification of the series resistance calls attention on an important aspect, namely the electron injection and trapping arise more massively underneath the accumulated drift region rather than underneath the back inversion channel.

4.3. Hot-carrier injection into the gate oxide

Another stress was performed by hot-carrier injection from the *front channel* ($V_{G1} = 3$ V, $V_{G2} = 0$ V, $V_D = 19$ V for 60 min). The back-interface parameters were not modified, implying that electron and/or hole injection into the BOX was irrelevant. The front-channel characteristics (Fig. 9b) are lightly affected by this type of stress. No significant changes were detected in subthreshold swing S_1, threshold voltage V_{T1}, and electron mobility μ_1. Only a slight current decrease is visible in strong inversion (Fig. 9b) even though the threshold voltage V_{T1} was not shifted. This mode of degradation is explained by the increase in series resistance due to electron injection primarily in the field oxide located above the drift region.

The comparison between front-channel and back-channel stresses denotes that the buried oxide is more prone to electron injection and trapping than the thin gate oxide.

4.4. Low temperature

The devices were operated at low temperature down to 77 K using a cryogenic chamber at the JPL. As expected, the front- and back-channel threshold voltages increase at 77 K by 0.25 and 25 V respectively (Fig. 10), whereas the subthreshold slopes are highly improved. A shift of $\Delta V_{T1}/\Delta T \approx 1.1$ mV/K mainly corresponds to the variation of the Fermi energy. Note that although the depletion depth extends in the body, the device continues to operate at 77 K in partial depletion mode.

The series resistance of the drift region versus back-gate bias, at 300 and 77 K, is illustrated in the inset of Fig. 10b. The series resistance is subject to two opposing factors: (i) increase of mobility (via reduced phonon scattering) which lowers the resistivity of the drift region and (ii) extension of the depletion depth which tends to increase R_s, except in region 3. There is no evidence for impurity freeze-out. For $-60 < V_{G2} < 20$ V, R_s exhibits a net increase at low temperature due to the predominant effect of widening of the depleted area in the drift region. When the drift region becomes accumulated, for $V_{G2} > 20$ V, the series resistance decreases at low temperature. In this mode of operation, the series resistance is only influenced by mobility enhancement, resulting in a decrease of resistivity and equivalent series resistance of the drift region.

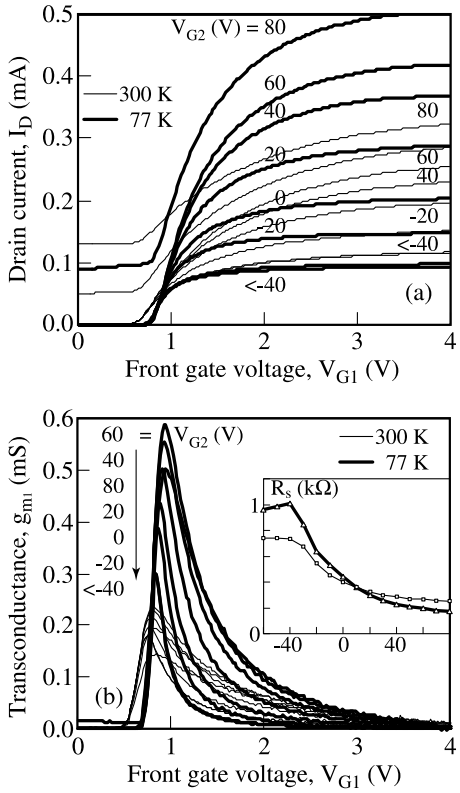

Fig. 10. (a) Drain current and (b) transconductance versus front-gate voltage for different back-gate biases, in a LDMOSFET operated at 300 and 77 K. The inset shows the corresponding variations of the series resistance with back-gate bias.

Fig. 10b shows that, as temperature is lowered, the transconductance is also governed by the increase in mobility and the variation of series resistance described above. The predominant effect is the mobility enhancement, resulting in a net increase of the transconductance peak by a factor 3. The lateral shift of the transconductance peak at low temperature follows the increase in V_{T1}. The variation of the transconductance with V_{G2} is qualitatively comparable at 77 and 300 K. The maximum value of the transconductance again is obtained just before the back channel is activated.

Fig. 10a shows that, irrespective of the threshold voltage increase, the drain current can be enhanced at 77 K by a factor of 2 (for $V_{G1} = 4$ V and $V_{G2} = 60$ V). This current improvement denotes the key roles played by the series resistance and carrier mobility.

4.5. Breakdown voltage

The breakdown voltage V_{BD} was defined as being equal to the drain voltage which yields a saturation

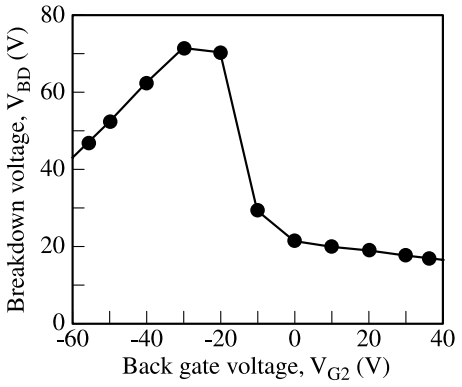

Fig. 11. Front-channel breakdown voltage versus back-gate bias in an n-channel LD-MOSFET ($V_{G1} = 0$ V).

front-channel current $I_D > 10$ nA, measured at $V_{G1} = 0$ V. Fig. 11 shows the typical variation of V_{BD} with back-gate bias. An excellent breakdown voltage, exceeding 70 V, is reached for $V_{G2} = -25$ V, when the drift region is depleted, but without having its film–BOX interface inverted yet. The series resistance is close to the maximum value which lowers the effective voltage drop V'_D on the channel. Since V_{BD} is governed by the breakdown of the parasitic bipolar transistor, a higher series resistance is the condition for improved breakdown in the LD-MOSFET. This is confirmed, at higher back-gate bias, where the lowering in V_{BD} (down to about 20 V) parallels the gradual reduction of R_s.

A different mechanism occurs at very negative back-gate bias. Although the series resistance is reaching the maximum value (see Fig. 7), the breakdown voltage degrades. For $V_{G2} < -25$ V, the bottom of the drift region becomes inverted whereas the back channel (in the body) is accumulated. A layer with a high density of holes is building up at the back interface. The field-induced p^+–n^+ junction, between the back-interfacial layer and the drain region, is responsible for direct tunneling which lowers the breakdown voltage.

The above results are quite general and can be applied to LD-MOSFETs with a higher breakdown voltage which can be achieved by using thicker film and BOX layers, and a longer, more resistive drift region [12–15]. These results also suggest that radiation will likely reduce the breakdown voltage of LD-MOSFETs.

5. Conclusion

Several types of device degradation, corresponding to extreme conditions of operation of SOI LD-MOSFETs, have been investigated and their effects have been compared. The degradation mechanisms are all captured by a universal model, which accounts for the modulation of the series resistance of the drift region. This modulation may take various forms according to the nature of the generated defects: (i) positive charge trapping in the BOX after irradiation, (ii) negative BOX charges after hot-electron injection from the back channel, (iii) hot-electron trapping in the field oxide after front-channel degradation, and (iv) extension of the depletion region combined with the mobility enhancement for low-temperature operation. The formation of defects during device degradation is rather equivalent to applying a pseudo-back-gate bias. Our model and supportive experimental data are useful for understanding the capability of SOI LD-MOSFETs to operate in harsh conditions, and also for optimizing the device architecture.

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